A State-of-the-Art Review on IC EMC Reliability

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Electromagnetic compatibility (EMC) of integrated circuits (IC) should be within the desirable level for maintaining the functional safety and reliability of electronic systems in different complex automotive and aeronautical applications. Throughout the operational lifetime of ICs, harsh environmental conditions including extreme high or low temperature, humidity, shock, and stress tend to cause intrinsic physical degradations, which results in significant variations of long-life EMC performance of IC device. Consequently, ensuring along with maintaining electromagnetic robustness (EMR) and integrating IC reliability throughout their whole lifetime period is a key challenge that needs to be addressed. The purpose of this paper is to conduct a comprehensive state-of-the-art study on developing accurate immunity and emission models of ICs focusing on quantitative evaluation of experimental characterization based on various IC EMC measurement methods under various ageing accelerated life tests. Producing accurate transient EMC models help not only estimate EMC immunity and emission levels of ICs but also allows determining different failure types and mechanisms due to radio frequency disturbance when applied to IC model structures. This paper presents a few recent researches on the conducted pulse immunity as well as emission models for ICs based on the IEC standard models, showcasing the electric fast transient (EFT) simulations and measurements applied on different IC pins considering the ageing impact. Previous studies demonstrated the importance of the ageing on the EMC performance of ICs depending on the ageing stress parameters. Future perspective of the current study would involve proposing and implementing predictive reliability model for the IC during its entire lifetime under accelerated life tests.

Keywords: EMC, electromagnetic robustness, reliability, integrated circuits, conducted immunity and emission model, EFT.

1. Introduction

Characterizing and determining complex EM immunity and emission issues of ICs under complex EM environment is essential for accurate evaluation electromagnetic compatibility (EMC) and reliability of ICs. The IC-EMC lifetime reliability metric refers to the function that can be expressed in terms of parameters to indicate or predict how long the system would be performing before exhibiting various EMC failures under different external operational ageing conditions. Adopting realistic and accurate model construction with precise model validation to predict EM immunity and emission performance of ICs have attained significant importance to IC designers and manufacturers. Evaluation of predictive EMC simulation results would be necessary to IC manufacturers for reduction of time, number of prototype cycles and fabrication cost prior to manufacture ICs.

Simulating immunity and emission models can help IC designers to understand and anticipate EMC levels to conducted harmonic disturbance when applied to IC pins, which in turn enable IC manufacturers to provide conclusive statement on whether IC would be EMC compliant prior to manufacturing. Moreover, EMC model construction and obtaining EMC results by simulations in various CAD software are considered very useful and easy to analyze compared to that of the IEC standard EMC measurement tests (IEC62132-4, 2003)-(IEC61967-4, 2006). Unique EMC immunity and emission model at device or component level would enable to determine different failure mechanisms and its origin due to injecting conducted EFT pulses or coupled high frequency RF (Radio Frequency) signals to induce EMI in different IC pins.

Numerous researches were conducted on developing EM immunity and emission models. Different types of immunity models for low dropout voltage regulator (LDO) were proposed and designed in CMOS 90nm technology (Wu et al., 2014). Those immunity models were compared

Proceedings of the 31th European Safety and Reliability Conference
Edited by Bruno Castanier, Marko Cepin, David Bigaud and Christophe Berenguer
 Published by Research Publishing, Singapore
ISBN: 981-973-0000-00-0 :: doi: 10.3850/981-973-0000-00-0 esrel2021-paper

to experimental results for highlighting importance of including PCB track model, on-chip package, decoupling and parasitic components network to design the IC model with greater accuracy. Moreover, immunity behavior of digital cores embedded in an IC designed in 0.18 µm CMOS technology was studied and evaluated using the developed immunity model involved construction and extraction of different components including PCB track model, IC package and lead model, direct power injection (DPI) immunity test setup model and transistor based model for digital cores (Alaeldine et al., 2008).

In order to predict impact of ageing under accelerated lifetime operating conditions (stress magnitude and durations) on the EMC level and identify origins of different types of failure induced to aged components, ageing model and conditions have been integrated to proposed ageing-aware immunity and emission models. Susceptibility models proposed for operational amplifier (Huang et al., 2015) designed in 65 nm CMOS technology included aged transistor netlist models to simulate and predict susceptibility evolution before and after ageing conditions applied on the electrically stressed power supply voltage at different stress durations. Furthermore, researchers also produced quantitative estimated ageing analysis based on aged immunity models for voltage regulator (Wu et al., 2013) and bandgap voltage reference (Hairoud-Airieau et al., 2017) at component level could analyze EM susceptibility to harmonic disturbance coupled on power supply pins before and after ageing in frequency domain.

This research paper aims to provide a comprehensive review on immunity and emission model construction, extraction and report analysis on results obtained from validation of those proposed models illustrated in some of the previously conducted research works. This paper considers few relevant case studies on EMC modeling approach including the ageing impact that are more reliable, essential and closely related to the ongoing research interest. Note that, due to the limited page number, certain previous literatures have been considered to fulfil the research goal of this manuscript. The paper is organized as follows. Section 2 presents detailed description on EM immunity modeling methodology, whereas Section 3 deals with the emission modeling technique and the outcome of findings demonstrated in research studies. Section 4 discusses the impact of ageing on immunity and emission models and explain the origin of the findings predicted by introducing ageing model into the developed immunity and emission level. Section 5 summarizes the findings of those research works including the future perspective of the current study in terms of proposing lifetime reliability model for ICs with certain functionality to predict EM immunity evolution with time under ageing conditions.

2. EM IC Immunity Modelling Methodology

The basic integrated circuit immunity model (ICIM) structure of an IC chip to coupling of conducted harmonic disturbance on various input/output pins, power supply (Vdd) and ground pins (GND) is based on readily available ICIM-CI standard proposal based on standard IEC 62433-4 (Marrot and Levant, 2008). Airieau et al., (2016) proposed dual port ICIM-CI model structure for conducted transient EFT pulse applied on different IC pins shown in Fig. 1. That model composed of passive power distribution network model (PDN) that consists of passive lumped resistive, inductive and capacitive components for modeling the path way of EM interference injected at different disturbance input (DI 1 and DI 2) terminals of IC. It consists of internal behavioral blocks (IB) that represent different circuit schematic

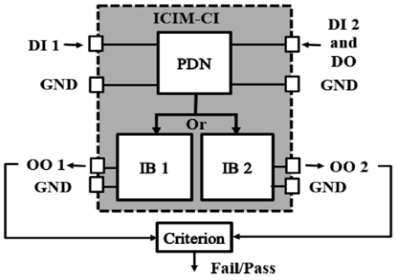

Fig. 1. Dual port ICIM-CI model structure of an IC (Airieau et al., 2016).

schematic embedded in the IC. Applying failure criterion to different observable outputs (OO) pins of the IB blocks would allow identifying the IC failure types and immunity level to conducted interference associated to different output waveform observed at those output pins. The conducted immunity model construction and extraction measurement techniques have been mentioned in the following sub-sections along with the model validation results and analysis on the IC immunity modeling.

2.1. ICIM construction

IC conducted pulse immunity model (ICIM-CPI) was proposed for a 32-bit microcontroller that included EFT test bench setup model to characterize immunity behavior according to the standard (IEC 61000-4-4 standard). Durier and Fernandez-Lopez (2018) proposed a block diagram to represent the overall ICIM-CPI model construction of the microcontroller as shown in Fig. 2.

The overall immunity model structure is composed of PDN block that is be used to represent overall impedance between the EFT injected pulse terminals (T1 and T2) and reference ground terminals (GND1 and GND2). PDN model was designed and constructed using linear passive components (resistors, inductors and capacitors) in series-parallel connections to model IC package and lead, on-chip interconnections and IC bonding wires to connect between VDD and GND pins.

The purpose of designing the PDN block is to model conducted disturbance coupling path from the external EFT model environment to the internal IC pin. Non- linear block (NLB) model design was performed with non-linear active electronic components such as diodes to protect the IC from the permanent failure or damage due electrostatic discharge (ESD) coupling and EFT pulse injection to IO, VDD and VSS pins. NLB model is essential to describe non-linear characteristics of the EFT pulse propagation pathway into the IC and was linked with PDN model through internal terminals (i.e. IT1) and to connect VDD with input terminals of IC as shown in Fig 2. The output waveform was

monitored at the output observable (OO) IC pin due to the EFT pulse injection at T1 terminal. The failure block contains files or computed data or results obtained at OO terminal, which allows detecting the failure types due to injected harmonic disturbance depending on the failure criterion defined at the associated output pin.

The CI model of an 8-bit microcontroller was developed for simulating immunity behavior in time- domain based on experimental characterization of EFT test setup (Zhang et al., 2014). The overall IC immunity model considering EFT

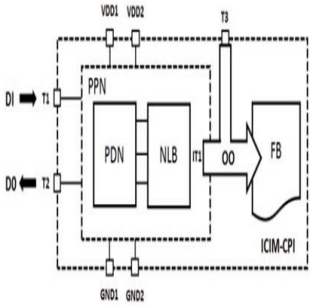

Fig. 2. Structure of the proposed ICIM-CPI model (Durier and Fernandez-Lopez, 2018).

test setup model, PDN, IO model and EFT or ESD protection model within the IC package and die (Fig. 3) (Zhang et al.,2014).

The overall IC immunity model construction involved modeling EFT test bench using transient voltage source with a 50-Ω series resistance for producing standard EFT pulse, followed by a voltage amplifier to amplify EFT generated voltage up to 2 kV. In order to model the EFT disturbance between the EFT source and IC pins, coupling paths were modeled using injection capacitor (Cinj) and DC power supply feed inductors as shown in Fig. 3. The high impedance between the VDD/VSS pins and IO pins was modeled using resistors (R2, R3) and capacitors (C2 and C3), respectively. PDN model was constructed using linear passive RC components connected in series-parallel networks for linear coupling between VDD/VSS pins and some non-linear active diodes for non-linear coupling between power and ground rails. PDN model, on-chip package model, IO model and ESD protection model was developed from the IC immunity experimental characterization, basic knowledge of IC layout structure and IC manufacturer provided data could be obtained from for EFT protection structures (Stockinger et al., 2003). EFT protection model could be obtained based on the IC layout design from the IC manufacturer that consist of diodes that should function as trigger, nFET and pFET power clamps.

This IO protection model circuitry was implemented with each IO pad or pin to allow diverting large currents from the VDD pins to the GND during EFT events and to prevent rapid or sharp rise or change in voltage of VDD under coupling of EFT pulse (Zhang et al., 2014). The transistor-netlist based circuit model for the IO cell in Fig 4 (Zhang et al.,2014) is composed of nFET and pFET transistors so that the IO cell can be used both as high or low enabled input and output. Different measurement ways to extract parameters of constructed PDN, IO and lumped parasitic components of series-parallel network on-die package model will be discussed in the next subsection.

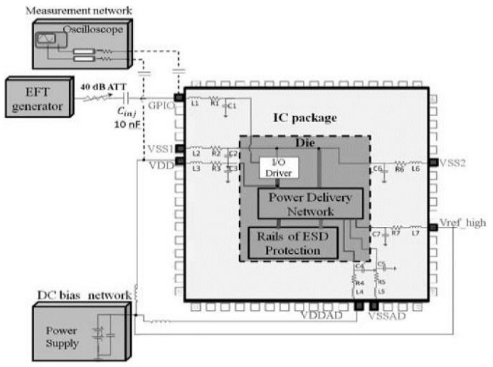

Fig. 3. IC model structure with EFT setup (Zhang et al., 2014).

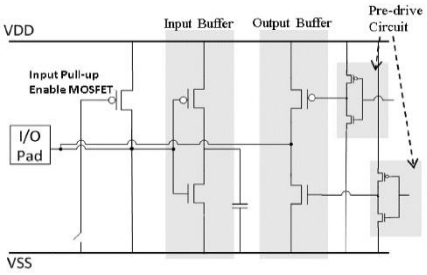

Fig. 4. IC model structure with EFT setup (Zhang et al., 2014).

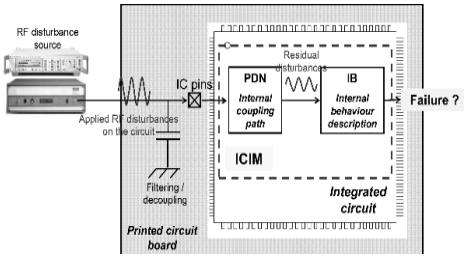

Fig. 5. IC immunity model for the PLL component including the DPI test setup (Boyer et al., 2012).

Research study was also conducted to construct conducted immunity model of the PLL embedded in the IC designed 90 nm CMOS technology in order to estimate the long-term conducted susceptibility of the PLL in frequency domain due to the injection of conducted harmonic disturbance power to the VDD pin of the IC (Boyer et al., 2012). The simplified IC susceptibility model diagram for predicting the PLL immunity with DPI setup is presented in Fig. 5 (Boyer et al., 2012). The proposed susceptibility model for the PLL include model construction two main blocks. PDN model for the PLL circuit structure was designed with passive linear R, L and C components to demonstrate the overall equivalent impedance network between the VDD and GND pins for each different sub-blocks of the PLL. The PDN model included on-chip interconnection, parasitic inductance for the IC package along with the DPI test bench model and EMC test board model for explaining exact EMI coupling paths to different pins of PLL structure. The objective of the IB model construction for the PLL is to explain and understand the PLL circuit response to the conducted harmonic disturbance coupled on the VDD pins of different sub-circuit blocks (i.e. frequency divider, voltage controlled oscillator and phase detector). IB block model was constructed from using the

transistor based SPICE model to design the complete PLL circuit schematic in bulk CMOS technology. Accurate IB block model description could enable to detect the failures induced by the EMI coupling on the VDD pins, which results in validating the immunity model by producing the simulated immunity curve comparable to the experimental results.

2.2. ICIM extraction

IC Immunity model extraction involves determining parametric values of different linear and non-linear components that has been used to construct different parts of the model. The research study presented by Boyer et al., (2012) extracted PDN block model for the PLL circuit from impedance measurements by *S*-parameter experimental characterization using 2-port vector network analyzer (VNA) and high frequency probes. Different types of impedance measurements between the VDD and VSS pins of the PLL circuit enabled to extract exact component values for the package inductance, equivalent capacitance and determine substrate-coupling measurement values.

Similarly, *S*-parameter experimental measurement technique was also used for impedance measurements between each VDD and VSS pins to extract both on-chip package lumped parasitic component values and passive linear components of the on-die PDN model constructed for an 8-bit microcontroller. EFT/ESD protection network model could be extracted from the I-V graphs produced by the experimental measurements of current (I) and voltage (V) for non-linear active EFT and ESD protection diodes. IO cell model extraction, which depends on the type of cell configuration (logic high or low output), could be achieved by certain experimental test setup for obtaining nFET and pFET parameters, including gain, voltage and current values (Zhang et al., 2014).

Different ways to determine impedance between different IC pins by *S*-parameter measurements were proposed for determining the package inductance and capacitance values. Fig. 6 shows one of the possible measurement technique for determining the impedance between the power rails of IC and package inductance of bonding wires (Zhang et al., 2010). This measurement method allows to measure S_{11} parameter, which could be used to determine the input impedance and hence extract the R6, C6 values as indicated by the arrows marked the on-die PDN model as shown in Fig. 6.

The study conducted by Zhang et al., (2010) suggested another *S*-parameter measurement method using VNA was proposed for determining capacitances between IC package, die and VDD/VSS planes. That measurement method involved connecting one port of the VNA to any one pin and the other port to the GND for measuring S_{11} parameters while other IC pins remain disconnected as depicted in Fig. 7 (Zhang et al., 2010). This measurement method allows to obtain L1, C1 and R1 values. Hence, experimental characterization are necessary to compute and extract the parameters of different components used to develop the immunity model.

The non-linear block (NLB), consisting of active diodes and I/O ESD/EFT protection models, could be developed and extracted either from the IBIS file or by

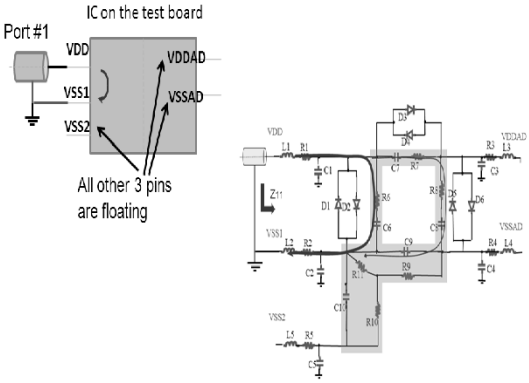

Fig. 6. Measurement method for the IC PDN model extraction (Zhang et al., 2010).

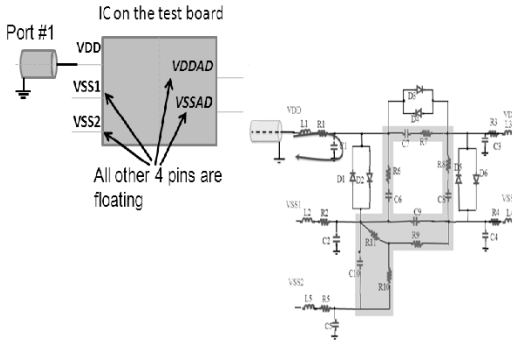

Fig. 7. Measurement method for IC package model extraction (Zhang et al., 2010).

simulation using a circuit simulator based on the knowledge of the specific IC modeled by the user. The Transmission Line Pulse (TLP) measurement approach is performed using the TLP generator based on the IEC 62615 standard for obtaining I/V measurements to extract the NLB components model (Durier and Fernandez-Lopez, 2018). Injection of the TLP pulse at different input terminals and measuring voltage and current values at these terminals would allow characterizing active diodes connected between GND and input terminals.

2.3. ICIM validation

After completion of the PDN and IB block model design, construction and extraction steps, conducted ICIM validation is very crucial to proof accuracy of the developed immunity model. Model validation step involves conducting EMC performance simulations in different CAD software so that the simulation results of predictive EM susceptibility level can be comparable to actual measurements obtained from available experimental immunity characterization tests. The developed conducted immunity model of an 8-bit microcontroller was simulated and the results were compared with experimental data. Fig. 8(a) illustrates the simulated curve for the predicted voltage variation waveform and actual measurement waveform when an EFT voltage of 200 V was injected into VDD pins of the IC (Zhang et al., 2014). Time-domain immunity characteristic of both simulated and measured graphs demonstrates similar trend in the VDD variation with minimal difference, which proves the validity of the proposed model for estimating and understanding IC

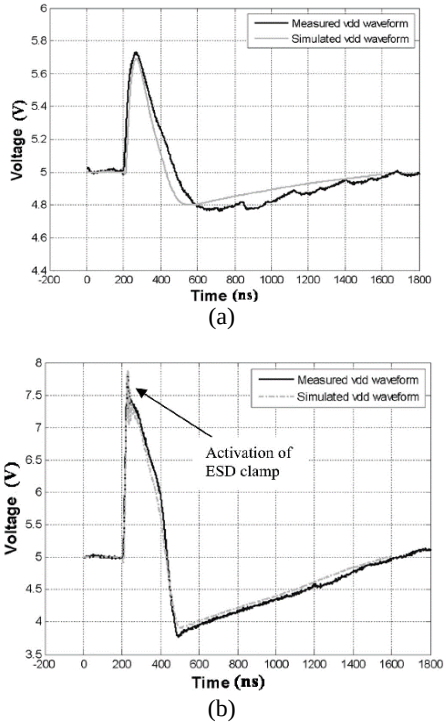

Fig. 8. Model validation result (a) EFT voltage 200V (b) EFT voltage 1600 V applied to the VDD pin (Zhang et al., 2014).

immunity issues. The developed model was further analyzed with ESD diode model by changing the VDD waveform due to coupling of 1600 V EFT voltage into the VDD pin. Fig. 8(b) demonstrates a sharp rise in the VDD voltage in the form of a spike followed by rapid decline of the supply voltage within very short time interval. The peak value is directly related to the applied EFT voltage leads to trigger the non-linear active diode so that the high current generated on the VDD pin could be diverted through the diodes from the VDD to the GND for ensuring protection of the IC pins from permanent damage.

The conducted immunity model for the PLL was constructed, extracted and simulated for *S*-parameter measurements to proof that the equivalent input impedance of the extracted PDN block is similar to that of experimental measurements over the whole frequency range. Impedance (Z_{11}) comparison profile diagram for the VCO sub-circuit block of the PLL circuit is shown in Fig. 9 (Boyer et al., 2012). Comparing impedance magnitude of both simulated and measured curves depict that the impedance matches with little variations over the entire simulated frequency range up to 1 GHz.

Followed by the validation of the PDN model extraction, the complete PLL immunity model was simulated in transient condition to obtain power supply voltage fluctuation at different incident RF power and frequency induced by the EMI coupling on the VDD pins. Considering the immunity failure criterion (e.g. 10% voltage variation of the nominal VDD supply) applied at the output of the developed model, minimum threshold injected power (in dBm) and corresponding frequency (MHz) could be recorded over the entire frequency range between 1 MHz to 1 GHz. The immunity curve of the power injected against the incident frequency of the harmonic disturbance causing the immunity failure is presented in Fig. 10 (Boyer et al., 2012).

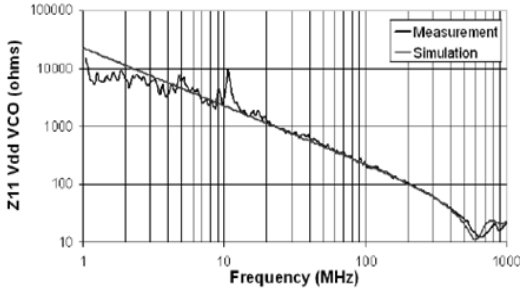

Fig. 9. Impedance measurement from VDD VCO pin (Boyer et al., 2012).

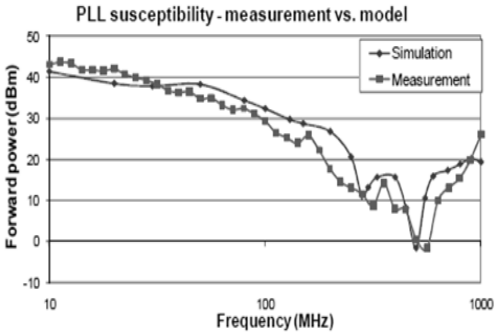

Fig. 10. Immunity profile comparison between the model and measurements (Boyer et al., 2012).

Comparing the estimated immunity curve in frequency domain with the experimental measurement of susceptibility level show that the model accurately predicted the susceptibility level over the entire frequency range. Fig. 10 also shows that high susceptibility at frequency of about 400 and 800 MHz could be determined using the developed model, with slight overestimation of immunity level in the low frequency range.

3. Integrated Circuit Emission Model: Construction, Extraction and Validation

EM emission model of an IC can be produced and developed by relying on the simple standard ICEM model approach (IEC 62433-2, 2006). The conducted EM emission model for the digital core circuit embedded in the IC was developed (Boyer et al., 2013a). The emission model consisted of the PDN block model construction that is similar to the immunity model. However, unlike the IB block model, the internal activity (IA) block model should be constructed and included to develop EM emission model. In order to develop the IA block model, two current sources were used in parallel connection for quantifying the current generated from the digital core circuit activity during the EM emission (Fig. 11) (Boyer et al., 2013a). Two current sources were used to represent the IA block model that could produce triangular waveform during simulations. The IA model parameters include rise time, fall time and peak current, which could be extracted from the SPICE transient simulation of the digital core circuit followed by tuning the parameter values for obtaining best fit simulated current

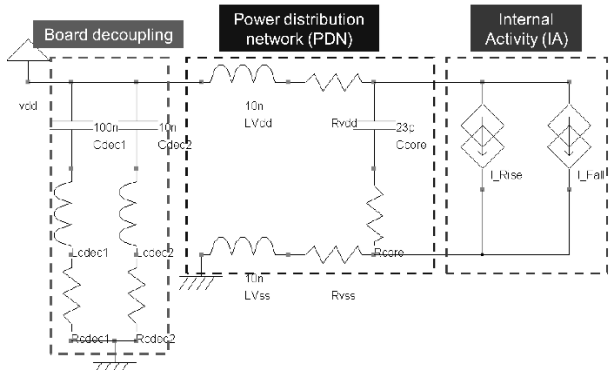

Fig. 11. Emission model structure for the digital core circuit embedded in the IC (Boyer et al., 2013a).

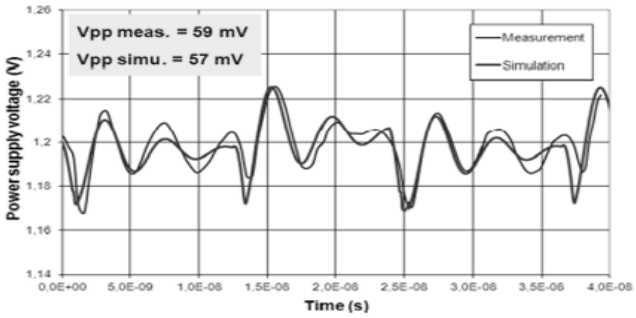

Fig. 12. Simulated and measured digital core power supply voltage fluctuation (Boyer et al., 2013a).

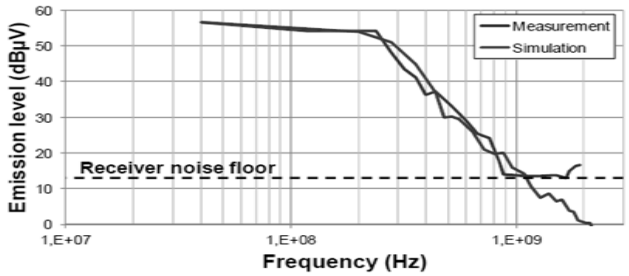

Fig. 13. Simulated and measured conducted EM emission level from the digital core (Boyer et al., 2013a).

waveform with respect to the actual current waveform. The proposed PDN network, composed of package inductance and resistances between the VDD and VSS pins along with decoupling capacitance for the core, could be extracted from the *S*-parameter measurements followed by tuning linear passive R, L, and C component values until best fitting the impedance profile obtained in measurements between the VDD and VSS pins of the digital core.

The emission model validation produced simulation results on the VDD supply voltage fluctuations of the digital core activity during the EM emission, which was compared to the measured values, as shown in Fig. 12 (Boyer et al., 2013a). Analyzing and evaluating the simulation results depict similar change in the VDD core voltage fluctuations due to the EM emission, resulting comparable peak-to-peak voltage and oscillating time period. The EM model was simulated to produce the emission level curve as illustrated in Fig. 13 (Boyer et al., 2013a) in frequency domain. The simulated EM emission level is comparable to measured results and follows similar decreasing trend with increasing frequency of the applied harmonic disturbance. However, slight mismatch in the emission level at high frequency between the measured and simulated results was noticed. Improving and minimizing the difference between the simulated and measured results require designing and constructing the complex PCB board and substrate coupling models together with the extraction of complex triangular waveform from the IA block using precise power consumption analysis of the digital core.

4. Ageing-aware Immunity Model of ICs

The effect of ageing on the EM immunity or emission level of ICs at device or component level under influence of different external factors (electrical stress, high or low temperatures) applied for certain stress durations can be modeled to analyze, predict and evaluate long-term evolution of EMC performance. Fig.14 presents the proposed block diagram with external environment model integrated into the standard conducted ICIM-CI model for conducting ageing analysis to evaluate variations of EM immunity levels of electronic components (Dubois et al., 2015). Temperature is one of the external factor considered in the environment model, which acts as the ageing stress factor for the Opamp at the component level. The environment model was introduced in the ICIM-CI model to study the ageing impact on the EM susceptibility level.

Introducing ageing effect into the immunity or emission model enables to understand and analyze the origin of ageing impact on the EMC performance evolution and detect causes of different failure types. Based on the suggested block diagram provided in Fig.14, the flowchart proposed in Fig. 15 explains how to develop the ageing model based on ageing conditions and how this ageing model should be incorporated with the developed immunity or emission model.

The first required step is to conduct transient simulation on SPICE transistor model under ageing conditions for identifying aged transistors. This is due to the intrinsic degradation mechanisms followed by computing aged transistor parameters (i.e. mobility and threshold voltage) values. After identifying the aged transistors, the aged transistor model is developed and extracted by either experimental device characterization or including the new electrical parameter values computed analytically during ageing (Boyer et al., 2012). Aged transistor model netlist can be included in the simulation library to construct immunity model containing aged transistor model. Immunity model simulation then produces the EM immunity curves after applying ageing conditions.

4.1. Ageing impact model validation on EMC

The simplified block diagram of the conducted susceptibility model was developed for an operational amplifier in the negative feedback configuration with unity gain to conduct ageing analysis (Fig. 16) (Huang et al., 2015). The simplified EM susceptibility model includes aged transistor netlists for the IB block model in order to evaluate the effect of the applied ageing conditions (electrical stress supply voltage, stress duration). Before including aged transistor netlist in the developed model, variation of the threshold voltages and mobility were

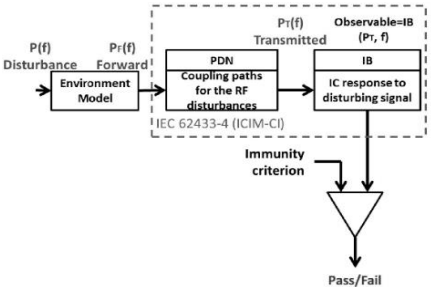

Fig. 14. Block diagram for the ICIM-CI model with integrated external environmental model for ageing (Dubois et al., 2015).

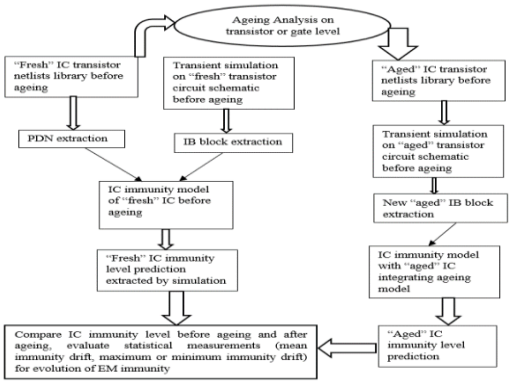

Fig. 15. Proposed ageing-aware ICIM model methodology.

experimentally characterized for transistors when electrical stress voltage was applied to the biasing voltage stress durations. Acceleration of transistor degradation mechanisms (i.e. hot carrier injection, negative bias transistor instability) due to ageing was considered as the main reason for variations of these electrical parameters.

Offset voltage output induced by the conducted EM interference at a constant injected frequency of 200 MHz and injected RF power increasing from 2 to 5 dBm at different aged time duration is depicted in Fig. 17 (Huang et al., 2015). The graphical results show an increase of DC offset output voltage with the increasing stress time. Moreover, predicted EM susceptibility also increases with the increasing stress duration and injected RF power. The reason for such trend could be explained due to the acceleration of the intrinsic degradation mechanisms that can be responsible for incrementing threshold voltage according to stress magnitude and duration.

Emission model developed for the digital circuit designed in 90 nm CMOS technology was electrically stressed up to a given stress time. Ageing-aware emission model produced after determining the analytical relationship between threshold voltage (Vth) variation and stress duration for different applied stress voltage. Threshold voltage variations of the proposed emission model is shown in Fig. 18 (Boyer et al., 2013b). The graph shows the best-fit curve for the model on the experimentally characterized measured value and increase of the Vth would be acceptable according to the nth power MOSFET law (Dunga et al., 2007). Because of the increase in the threshold voltage with the stress duration, the current consumption modeled by the IA block parameters for the digital core activity could also vary. Consequently, the aged IA block included new parameters (i.e. rise time, fall time, peak current) while considering the

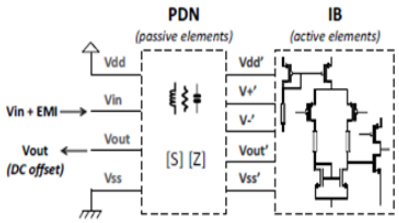

Fig. 16. Proposed ageing-aware EM susceptibility model structure of the operational amplifier (Huang et al., 2015).

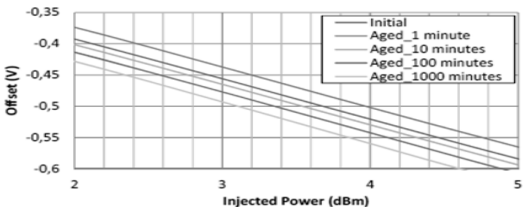

Fig. 17. Ageing impact on the DC offset voltage as a function of the RF power at 200 MHz (Huang et al., 2015).

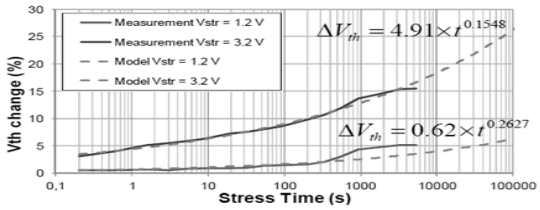

Fig. 18. Threshold voltage variations depending on the different ageing conditions (Boyer et al., 2013b).

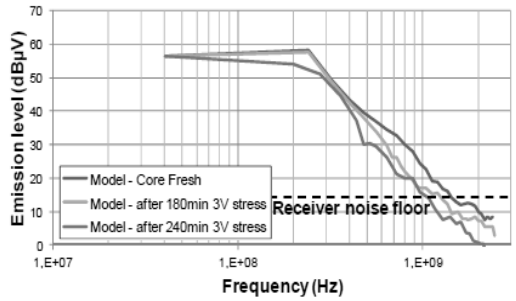

Fig. 19. Evolution of the EM emission level of the digital core circuit due to ageing stress (Boyer et al., 2014).

Vth variations with ageing stress conditions. The evolution of the EM emission level after ageing is provided in Fig. 19 (Boyer et al., 2014) after applying 3.6 V electrical stress voltage applied on the VDD pin for 120 minutes. Emission level declines with the increase of the injected RF frequency after ageing, which was likely due to the decline of the current generated from the digital core circuit switching activity and increase of the threshold voltage (Vth) of the aged transistors due to the activation and acceleration of the NBTI degradation mechanism. The NBTI degradation mechanism is activated under aged conditions when negative bias voltage at the gate-source terminal of the transistors and high RF voltage amplitude is applied on the VDD supply voltage.

5. Conclusion and Future Perspective of the Work

The main purpose of this extensive review research based paper is to conduct detail study on how to design, extract

and produce conducted immunity and emission models that would be based on the IC functionality and its applications. Several case studies were investigated to explain the modeling methodology for conducted model construction and extraction while considering conducted harmonic EMI applied on the IC pins. These developed immunity and emission models were validated up to a greater accuracy by comparing quantitative predicted EMC simulated results to that of experimental measurements. Moreover, a comparative analysis between the EMC model and measurements results could provide research insight on the importance of proposing complex IC EMC models, which include both PCB and the substrate coupling model for accurately predicting the susceptibility level over the higher frequency range greater than 1 GHz. It was also demonstrated how to conduct ageing simulations on conducted immunity and emission models to predict origin of the EMC performance degradation due to the intrinsic failure mechanism of ICs. However, these research works were only able to demonstrate EMC levels after certain ageing period, but not real-time monitoring of the ageing impact on EMC behavior of an IC.

The future perspective of this ongoing research work would involve proposing and developing predictive reliability model that could be integrated with the proposed unique conducted immunity model for addressing ageing induced EMC variations with time continuously. Predictive reliability model would be developed based on M-STORM (Multi-phySics mulTi-stressOrs predictive Reliability Model) along with consideration of M-HTOL (Multi High Temperature Operating Lifetime) accelerated ageing methods (Ghifri et al., 2019) for predicting different possible failure modes of ICs. Prior knowledge of these previously conducted research works would allow to understand the complexity in the immunity modeling techniques and helps to analyze the EMC simulated results both in time-and frequency-domain.

Acknowledgement

The work presented here is carried out in the framework of a thesis in co-supervision between the LARIS laboratory of the University of Angers and the ESEO of Angers. This research is co-financed by the Pays de la Loire region and the University of Angers.

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